

# System Level Estimation of Interconnect Length in the Presence of IP Blocks

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## Abstract

*With the increasing size and sophistication of circuits and specifically in the presence of IP blocks, new wirelength estimation methods are needed in the design flow of large-scale circuits. Up to now, the proposed techniques for wirelength estimation in the presence of IP blocks approached this problem either in a flat framework based on the geometrical structure of the circuit or in a hierarchical framework based on uniform distribution property for standard cells. In this paper, we propose a technique for hierarchical derivation of wirelength estimation in the presence of single and multiple blockages using Rent's parameter of the circuit by assuming non-uniform probability distribution for standard cells. To measure the accuracy of our estimation, we compared our results with the results of placement and routing using a commercial CAD tool. The results illustrate that in the presence of multiple IP blocks, the average error of our technique is less than 8%, as compared to its counterparts with the average error of 35% and 150%.*

## Keywords

Wirelength Estimation, Rent's Rule, Hierarchical Placement, Large-scale Circuits, IP Blocks, Non-Uniform Probability Distribution

## 1. Introduction

Computer-aided design flow is experiencing the trend of combining front-end floor-planning and back-end physical placement, which is indeed necessary to achieve more efficient designs. In this process, a fast and yet accurate estimation of system parameters such as power, clock frequency, and wirelength is critical to provide the front-end tool with accurate-enough information to adjust the early design decisions before proceeding deep in the design flow.

Early work on wirelength estimation is based upon an empirical model known as Rent's Rule [4]. Rent's Rule correlates the number of signal input and output terminals  $T$ , to the number of gates  $C$ , in a random logic network as  $T=AC^P$ .  $A$  is often called Rent coefficient, which is the average number of pins per cell. The Rent exponent,  $P$ , is the feature parameter of the circuit [5] which determines its complexity. The higher the Rent exponent, the more complex a circuit is. Using Rent's Rule, the first work on wirelength estimation is done by Landman and Russo [6] which was later improved by Donath [2]. [10] presented a new analysis of Donath's model that yields the length distribution functions of the interconnection at both the hierarchical level and system level. More recent work improves the estimation by considering non-uniform probability [7, 11] or recursively applying Rent's rule on an entire monolithic system [8].

Most of the research done on wirelength estimation is based on regularly placed circuits such as standard cell designs. With the trend toward IP-block-based design, macro cells as *blockage* (sometimes referred to as *obstacle*), are more likely to be present in the circuit [3]. The blockage may be an on-chip memory, analog or RF blocks, or pre-designed hard IP. The presence of the blockage may significantly increase wirelength and cause congestion [3]. Since the presence of blockage makes the traditional wirelength estimations far from reality, new techniques should be derived to address the problem of wirelength estimation. The first work on the wirelength estimation in the presence of obstacles has been done by Cheng

et. al. [3, 9]. In [3], the authors identified two distinct effects of obstacles on interconnection length: (1) changes due to the redistribution of interconnect terminals and (2) detours that have to be made around the obstacles. Theoretical expressions of both effects for two-terminal nets have been derived in a flat framework based on geometrical characteristics of the circuits. In [9], the authors represent a more complicated analytical model using a polynomial generation technique considering the layout region aspect ratio and the presence of the blockages. Their work, however, does not consider the complexity of the circuits into account and hence the average wirelength obtained from these techniques overestimate the actual wirelength for circuits with large chip area. In their method as long as two circuits have the same chip area, number of IP blocks and geometrical parameters for the IP blocks, they result in a unique estimation for the length of wire for both circuits, even though these two circuits may have different number and characteristics for standard cells and interconnections. Another work has been done in [1] which is an extension to Donath's hierarchical method for considering the effect of IP blocks. The major plus of this work is to consider the complexity of circuit (measured by its Rent exponent) in its analysis along with geometrical characteristics of the circuit. But, its main drawback is that it assumes a uniform probability distribution for all the standard cells which is not a realistic assumption.

In the current research, starting from Donath's hierarchical technique [2], his approach is extended to be able to consider obstacles in the placement area. It is shown how to derive a closed form expression for the total wirelength in the cases that the chip area includes either a single blockage or multiple blockages. In this work, we assumed a non-uniform probability distribution for standard cells over non-blocked parts of the circuit which was shown to be an accurate model for circuits in the real world [7]. Simulation results on the large circuits confirm that, in the presence of the obstacles, this technique is more suitable to estimate the wirelength than non-hierarchical techniques or techniques with uniform probability assumption.

The remainder of this paper is organized as follows. In Section 2, our methodology is explained. While Sections 3 and 4 present a theoretical analysis of average wirelength in the presence of single or multiple obstacles, Section 5 shows the experimental setup and simulation results of the proposed technique. Concluding remarks and future work are presented in Section 6.

## 2. Methodology

Similar to [1, 2], our technique to estimate the average wirelength is based on a top-down hierarchical placement of the circuit into a square Manhattan grid in the presence of obstacles. The circuit is partitioned hierarchically into four sub-circuits. This hierarchical partitioning is continued until the number of the standard cells in all of the sub-circuits is equal to or less than  $\beta$ , where  $\beta$  is a predefined constant. At each level of hierarchy, we deduce the average number  $n_h$  of interconnections and the average length  $r_h$  of interconnections between each two sub-circuits belonging to the same  $(h+1)$  level of hierarchy, but different  $h$  level of hierarchy.

Given the above model for the circuit, the feature parameter of the circuit  $P$  which is given by Rent's rule, and the above partitioning scheme, we want to estimate the total interconnection length of the circuit in the presence of obstacles. This is done by calculating the average number of interconnections  $n_h$  and the average length of the interconnections  $L_h$  at every hierarchical level  $h$ . The total interconnection length over all hierarchical levels is

$$L_{tot} = \sum_{h=0}^H n_h L_h \quad (1)$$

where  $H$  is the finest level of hierarchy. Since at every step of partitioning, each sub-circuit is divided by four, and in the last level of hierarchy the number of cells inside each sub-circuit is less than the factor  $\beta$ , the number of levels can be extracted from,

$$H = \log_4 \left( \frac{C}{\beta} \right) \quad (2)$$

The average number of interconnections between the sub-circuits in each level of hierarchy has been extracted using Rent's exponent which is experimentally proven to be a good indicator of the complexity of the circuit [2].

Using a similar type of analysis as [3], the average length of interconnection between the sub-circuits is calculated in each level of the hierarchy. Then, using formula (1), we estimate the total wirelength by multiplying the average number of interconnections by the average length of interconnections for each level of the hierarchy and summing all these values over all the hierarchical levels.

### 2.1. Average Number of Interconnections at Each Level of Hierarchy

In [2], Donath showed that by apply Rent rule on each level of hierarchy, the average number of interconnections at each hierarchical level can be calculated from,

$$n_h = \alpha AC(1 - 4^{P-1})4^{L(P-1)} \quad (3)$$

where  $C$  is the total number of cells,  $P$  is the Rent exponent,  $A$  is the Rent coefficient and  $\alpha$  is the fraction of the number of terminals for all the interconnections in one level. The value  $\alpha$  is  $\frac{1}{2}$  if each net has just two terminals, and is somewhat greater than  $\frac{1}{2}$  but less than 1 for circuits with multi-terminal nets [2]. Parameter  $L$  shows the level of hierarchy.

### 2.2. The Average Length of Interconnections at Each Level of Hierarchy

To start analyzing average wirelength at each level of hierarchy, we need to make some assumptions and define some terminologies at first.

**Assumption 1:** To compute  $L_h$  we assume that all of the nets have two terminals. This simplification is based on the knowledge that these nets are much more than all the other nets in the circuit and that multi-terminal nets can be modeled as a collection of two-terminal nets [12]. The effect of multi-terminal nets is incorporated into our estimation by using higher values for  $\alpha$  in the calculation of the average number of interconnections  $n_h$  as shown in the previous section.

**Assumption 2:** We assume that the available routing layers are such that the blockages are obstructions for both placement and routing. This model is based on what commercial tools support for placement and routing of large-scale circuits.

**Definition 1:** In level  $h$  of hierarchy an *intra-bin* wire is a wire that its terminals belong to the same bin, i.e. same part of the chip area.

**Definition 2:** An *inter-bin* wire is a wire that its terminals belong to different bins in level  $h$  of hierarchy, but to one bin in the level  $(h+1)$  of hierarchy.

**Definition 3:** In the presence of the obstacles, the *transparent-block* wirelength,  $L_{TB}$ , is defined as the wirelength when the obstacle is assumed to be transparent and wires can pass through it. For two-terminal nets, transparent-block wirelength is the Manhattan distance between them.

**Definition 4:** *Detour wirelength*,  $L_{DT}$ , is the detour length needed in a routing wire in the presence of the obstacles. In other words,  $L_{TB} = L - L_{DT}$ , where  $L$  is the Steiner minimal length of the net such that no part of the wire is routed inside any of the obstacles.

Figure 1 shows the intra-bin transparent-block and detour definitions.

In the next two sections, we show how to obtain the average wirelength in each level of hierarchy in the cases that we have single blockage or multiple blockages in the chip area. For the case that there is only a single blockage, we describe the research done by [1] which assumes uniform probability distribution for standard cells and illustrate how to extend their method for non-uniform probability distribution to improve the accuracy of estimation. For the multiple blockages case we just describe our method which assumes non-uniform probability distribution for cells. It is shown how to derive transparent-block and detour wirelength for both intra-bin and inter-bin nets. Basically, the inter-bin average wirelength analysis is the one we need to use in our methodology. We introduce the analysis for intra-bin average wirelength to help us doing the analysis for inter-bin average wirelength. To obtain the average wirelength, we decompose it into three parts, namely transparent-block and detour in X and Y directions such that,

$$\bar{L} = \bar{L}_{TB} + \bar{L}_{DT}^X + \bar{L}_{DT}^Y \quad (4)$$

where  $\bar{L}_{DT}^X$  and  $\bar{L}_{DT}^Y$  are the average detour in X and Y direction and  $\bar{L}_{TB}$  is the average transparent-block wirelength.

## 3. Theoretical Analysis of the Average Wirelength with Single IP Blocks

In this section, first we describe the method used in [1] to analyze the average wirelength in the presence of a single blockage by assuming a uniform probability distribution for cells and then we illustrate our approach to extend it by removing this assumption.

### 3.1. Uniform Probability Distribution

#### A. Average Intra-bin Wirelength

If there is no obstacle in the bin area, the average intra-bin wirelength can be easily obtained from (5), as shown in [3].

$$\bar{L}_{intra}^{Uniform} = \frac{\int_0^M \int_0^M \int_0^N \int_0^N (|x_1 - x_2| + |y_1 - y_2|) dx_1 dx_2 dy_1 dy_2}{\int_0^M \int_0^M \int_0^N \int_0^N dx_1 dx_2 dy_1 dy_2} = \frac{N + M}{3} \quad (5)$$

where subscript "intra" denotes that the average is taken over all intra-bin nets, in contrast to the inter-bin nets which will be discussed later.

To obtain the average wirelength in the presence of an obstacle, let us assume the obstacle's center is at position  $(a, b)$  and its width and height are respectively  $W$  and  $H$  (see Figure 1). Note that in this case  $P_1$  and  $P_2$  must be placed outside of the obstacle, i.e.  $P_1, P_2 \in A - S$ , where  $A$  is the set of all the points inside the bin and  $S$  is the set of all the points inside the obstacle.

With the same type of analysis as for formula (5), we can calculate the average transparent-block wirelength [3],  $\bar{L}_{TB, intra}$ , as  $\psi_1(N, M, W, H, a, b) / \psi_2(N, M, W, H, a, b)$  where,

$$\psi_1(N, M, W, H, a, b) = \iiint_{P_1, P_2 \in A-S} (|x_1 - x_2| + |y_1 - y_2|) dx_1 dx_2 dy_1 dy_2 = \frac{1}{6} (2N^2 M^2 (N + M) + 2W^2 H^2 (H + W) - 6NMHW(N + M - 2(a + b)) - HW(MW^2 + NH^2) - 12HW(Ma^2 + Nb^2)) \quad (6a)$$

$$\psi_2(N, M, W, H, a, b) = \iiint_{P_1, P_2 \in A-S} dx_1 dx_2 dy_1 dy_2 = (NM - WH)^2 \quad (6b)$$

Basically, in equations (6a) and (6b), we get the integral over the non-blocked area of the bin. By that, we mean that the terminals can be everywhere except the blocked part of the bin, but the interconnections can pass through the blockage.

For analyzing the intra-bin average detour wirelength in vertical direction, we consider the detour value as a random variable. For a random variable we have  $E(Y) = E(Y|X) \cdot \Pr(X)$ ; so we have,

$$\bar{L}_{DT, \text{intra}}^v = L_{DT, \text{intra}}^v \times \Pr_{DT}^v \quad (7)$$

where  $L_{DT, \text{intra}}^v$  is the average detour in  $Y$  direction, given that a detour happens in that direction. In [1, 3] it was shown that

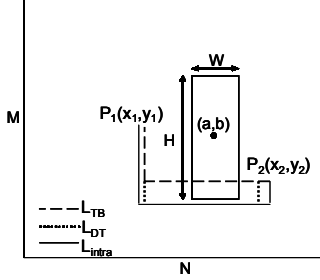


Figure 1: Definition of intra-bin transparent-block and detour wirelength.

$L_{DT, \text{intra}}^v$  is equal to  $1/3H$ . On the other hand,  $\Pr_{DT}^v$  is the probability of occurrence of the detour in that direction. Thus we have,

$$\bar{L}_{DT, \text{intra}}^v = \frac{2}{3}H \frac{H(N-a-W/2)H(a-W/2)}{(MN-WH)^2} \quad (8)$$

### B. Average Inter-bin Wirelength

According to Definition 2, a two-terminal inter-bin net is defined as a net with one terminal in a bin and the other terminal in the adjacent bin, either horizontally, vertically or diagonally. In the following, it is shown how to derive expressions for calculating average inter-bin wirelength in the presence of an obstacle for horizontally adjacent bins. The cases of vertically and diagonally adjacent bins are similar to horizontally adjacent bins and so omitted from this discussion for brevity.

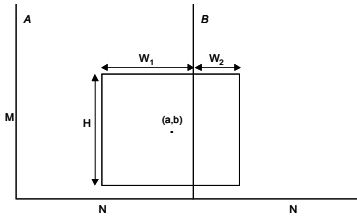


Figure 2: Two horizontal adjacent bins

#### B.1 Horizontally Adjacent Bins

Horizontally adjacent bins are shown in Figure 2. In this case, the average transparent-block wirelength can be computed as [1],

$$\bar{L}_{TB, \text{inter}}^v = \frac{\psi_1(2N, M, W, H, a, b) - \psi_1(N, M, W_1, H, a_1, b_1) - \psi_1(N, M, W_2, H, a_2, b_2)}{(MN - W_1H)(MN - W_2H)} \quad (9)$$

where  $W = W_1 + W_2$ ,  $b_1 = b_2 = b$ ,  $a_1 = a - W/2 + W_1/2$ , and  $a_2 = W_2/2$  and  $\psi_1$  is the same function as in (6a).

The average detour wirelength in  $Y$  direction can be expressed as,

$$\bar{L}_{DT, \text{inter}}^v = \Pr_{DT}^v \cdot L_{DT, \text{inter}}^v \quad (10)$$

where  $\Pr_{DT}^v$  is the probability of occurring a detour in  $Y$  direction which can be expressed as,

$$\Pr_{DT}^v = \frac{2H(N-a_2-W_2/2)H(a_1-W_1/2)}{(MN-W_1H)(MN-W_2H)} \quad (11)$$

This probability is equal to the portion of the area which a detour can occur divided by the non-blocked area of the two bins.

Moreover,  $L_{DT, \text{inter}}^v$  is the average detour length in  $Y$  direction given that a detour occurred in this direction. Similar to (8),  $L_{DT, \text{inter}}^v$  equals to  $1/3H$ . So, the average detour wirelength in  $Y$  direction can be extracted from (10) as,

$$\bar{L}_{DT, \text{inter}}^v = \frac{1}{3}H \frac{2H(N-a_1-W_2/2)H(a_1-W_1/2)}{(MN-W_1H)(MN-W_2H)} \quad (12)$$

The average detour wirelength in  $X$  direction can be found from,

$$\bar{L}_{DT, \text{inter}}^h = \Pr_{DT}^h \cdot L_{DT, \text{inter}}^h \quad (13)$$

where  $L_{DT, \text{inter}}^h$  can be calculated as,

$$L_{DT, \text{inter}}^h = \frac{4 \iint_{P_1 \in UA, P_2 \in LB} 2 \min(x_1 - (a_1 - W_1/2) + W_1', W_2 - x_2 + W_2') dx_1 dx_2}{2 \iint_{P_1 \in UA, P_2 \in LB} dx_1 dx_2 + 2 \iint_{P_1 \in LA, P_2 \in UB} dx_1 dx_2} \quad (14)$$

and  $\Pr_{DT}^h$  is the probability of occurring a detour in horizontal direction, which is equal to,

$$\Pr_{DT}^h = \frac{2(W_1(M-b-H/2)W_2(b-H/2) + W_1(b-H/2)W_2(M-b-H/2))}{(NM-W_1H)(NM-W_2H)} \quad (15)$$

Having had  $\bar{L}_{TB}^v$ ,  $\bar{L}_{DT}^h$  and  $\bar{L}_{DT}^v$  as the average transparent-block and detour wirelength of horizontal adjacent bins  $A$  and  $B$ ,  $L_h(A, B)$  in this case can be extracted from (4).

### 3.2. Non-Uniform Probability Distribution

In the technique discussed in the last section which was based on the Donath's method for analysis, every hierarchical level is treated separately with no knowledge of the length of interconnections from other levels of hierarchy. However, the optimal placement techniques try to place the interconnected blocks as close to each other as possible. In the hierarchical model, this means that an optimal placement technique will place blocks that are interconnected to a block of another square closer to the border of the two squares as shown in Figure 5. The previous technique does not consider this information.

**Definition 5:** We define the interconnection length distribution as the value indicates that for each length  $l$ , how many interconnections have this length. It was called the occupancy probability in [7].

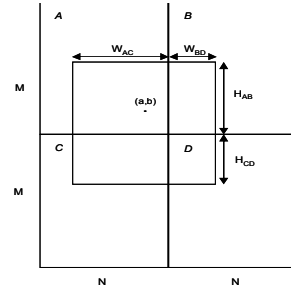


Figure 3: Bin A and D are diagonally and bin B and D are horizontally adjacent

According to [7] it can be seen that for all but nearest-neighbor nets ( $l = 1$ ), the power-law function of the form  $l^{-(4-2P)}$  can approximate the occupancy probability. This result was first reported in [2] and re-derived in [7, 8] using different techniques. This result suggests that, for any length of interconnection, the higher the length is the less the number of nets with this length can be, which reflect the behavior of the optimal placement.

#### A. Average Intra-bin Wirelength

Considering  $l^{-(4-2P)}$  as the occupancy probability of having a wire with the length of  $l$  instead of the uniform probability distribution, the estimation will be improved by multiplying this occupancy probability distribution by the structural probability distribution which we had before for the interconnection

estimation. So, the formula (6a) will be transformed to  $\bar{L}_{TB, \text{intera}}$  as  $\psi_1(N, M, W, H, a, b) / \psi_2(N, M, W, H, a, b)$  where,

$$\psi_1^{\text{non-uniform}}(N, M, W, H, a, b) = \iiint_{x_1, y_1 \in A-S} (|x_1 - x_2| + |y_1 - y_2|)^{-(3-2P)} dx_1 dx_2 dy_1 dy_2 \quad (16)$$

In order to solve this formula, according to Figure 4, there are 8 different regions for each of the two points  $(x_1, y_1)$ , and  $(x_2, y_2)$ . So there would be 64 different integrals to consider for solving formula (16). Let us define,

$$\delta = (|x_1 - x_2| + |y_1 - y_2|)^{-(3-2P)} \quad (17)$$

Consider the following equation,

$$\iiint_{x_1, y_1 \in A} \delta dx_1 dx_2 dy_1 dy_2 = 2 \iiint_{x_1 \in A-S, y_1 \in S} \delta dx_1 dx_2 dy_1 dy_2 + \iiint_{x_1, y_1 \in S} \delta dx_1 dx_2 dy_1 dy_2 + \iiint_{x_1, y_1 \in A-S} \delta dx_1 dx_2 dy_1 dy_2 \quad (18)$$

formula (16) is the last term of the above formula.

The first and third terms in the formula (18) can be easily computed by hand or by using Mathematica equation solver software. The Second term has 8 cases to consider, since the first point moves inside the non-blocked part which consists of 8 regions and the second point moves inside the blocked area which consists of 1 region. So, the number of integration is reduced to  $8 + 2 = 10$ . The formula for the case that the first point is in region 1 and the second point is in blocked area can be obtained from,

$$\psi_{(1,S)}(N, M, W, H, a, b) = \int_0^{H/2} \int_0^{H/2} \int_0^{W/2} \int_0^{W/2} (x_2 + x_1 + y_2 + y_1)^{-(3-2P)} dx_1 dx_2 dy_1 dy_2 \quad (19)$$

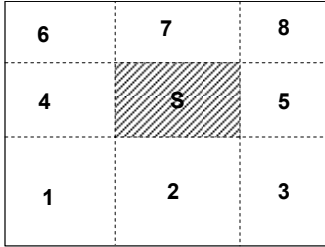


Figure 4: Integration regions for intra-bin transparent-block wirelength

And the formula for the case that the first point is in region 2 and the second point is in blocked area can be obtained from,

$$\psi_{(2,S)}(N, M, W, H, a, b) = \int_0^{H/2} \int_0^{H/2} \int_0^{W/2} \int_0^{W/2} (x_2 - x_1 + y_2 + y_1)^{-(3-2P)} dx_1 dx_2 dy_1 dy_2 \quad (20)$$

Because of the symmetry of the problem, the integration for all of the other regions can be calculated from (19) and (20) using different limits for the integrals.

Note that the denominator of the average transparent-block wirelength should be modified to,

$$\psi_2^{\text{non-uniform}}(N, M, W, H, a, b) \iiint (|x_1 - x_2| + |y_1 - y_2|)^{-(4-2P)} dx_1 dx_2 dy_1 dy_2 \quad (21)$$

on any specified region of integration.

### B. Average Inter-bin Wirelength

As it was shown in section 2, all of the formulas for inter-bin transparent-block part of the wirelength are using the formulas for the intra-bin transparent-block analysis. Having modified the formulas for transparent-block intra-bin wirelength, the formulas for transparent-block inter-bin wirelength can be extracted accordingly with no further analysis. In the next part we show how to extract detour inter-bin wirelength with non-uniform probability.

#### B.1. Horizontally Adjacent Bins

Let us consider Figure 5, for calculating the detour part of the wirelength. The behavior of an optimal placement necessitates having higher density of terminals closer to the middle border. A simple observation shows us that the non-uniform probability distribution of terminals does not have an effect on the vertical

detour of the points on the right and left sides of the obstacle, since the concentration of cells differs in  $X$  direction.

However, the non-uniform probability distribution has an effect on the horizontal detour of the points on the top and the bottom sides of the obstacle. The effect of non-uniform terminal distribution on the total horizontal detour in  $X$  direction given that a detour happens would be of the form of,

$$L_{DT,1}^{h, \text{non-uniform}} = \frac{4 \iint_{P_1 \in UA, P_2 \in LB} \iint 2\omega(x_1, x_2) \times (x_1 + x_2 + y_1 - y_2)^{-(4-2P)} dx_1 dx_2 dy_1 dy_2}{4 \iint_{P_1 \in UA, P_2 \in LB} \iint (x_1 + x_2 + y_1 - y_2)^{-(4-2P)} dx_1 dx_2 dy_1 dy_2} \quad (22)$$

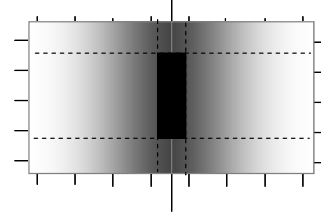


Figure 5: The optimal placement behavior in presence of blockage

where  $\omega(x_1, x_2) = \min(x_1 - (a_1 - W_1/2) + W'_1, W_2 - x_2 + W'_2)$ .

As it can be seen, solving the nominator of the above equation manually is difficult. Numerical equation solvers can always help in these cases.

## 4. Theoretical Analysis of the Average Wirelength with Multiple Blockages

The analysis of inter-bin average wirelength in the presence of multiple blockages can be performed by using the analysis for average wirelength in the presence of a single blockage. The inter-bin average wirelength for vertically and diagonally adjacent bins use the same type of analysis as horizontally adjacent bins and are omitted here for brevity.

### 4.1. Horizontally Adjacent Bins

As shown in Figure 6, in the presence of multiple blockages, similar to [3] the average transparent-block wirelength can be calculated from,

$$\psi_1 \left( A - \sum_i A_i, B - \sum_i B_i \right) = \psi_1(A, B) - \left( \sum_i \psi_1(A_i, B) + \sum_i \psi_1(A, B_i) - \sum_j \sum_i \psi_1(A_i, B_j) \right) \quad (23)$$

where,

$$\psi_1(A, B) = \iint_{x_1, y_1 \in A} \iint_{x_2, y_2 \in B} (|x_1 - x_2| + |y_1 - y_2|)^{-(3-2P)} dx_1 dx_2 dy_1 dy_2 \quad (24)$$

where  $(x_1, y_1)$  and  $(x_2, y_2)$  are the coefficients of the two points on every rectangular regions  $A$  and  $B$ , respectively.

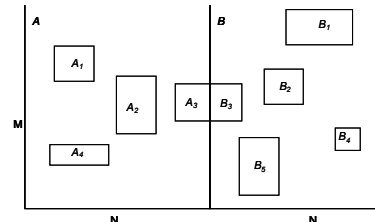


Figure 6: Horizontally adjacent bins with multiple blockages[1]

The average detour wirelength is more complicated in this case. If the obstacles do not overlap neither in  $X$  span nor in  $Y$  span, Cheng et. al. [3] showed that the effect of the obstacles on the average detour wirelength is additive and this problem can be treated as a combination of single blockage problems. But for real circuits this assumption seems to be too simplifying and it might overestimate the detour in some cases. Figure (7) illustrate this problem. The detour for the terminals inside region  $A$  and  $B$

equal to the maximum detour around  $A$  and  $B$  which is less than the summation of the detour for these two blocks. Instead we use a heuristic to estimate the amount of detour for this case.

**Lemma 1.** Every two disjoint blocks overlap at most in either  $X$  or  $Y$  spans. If two blocks overlaps in both spans, one covers all or part of the other one; so we decompose them to several blocks with no overlap.

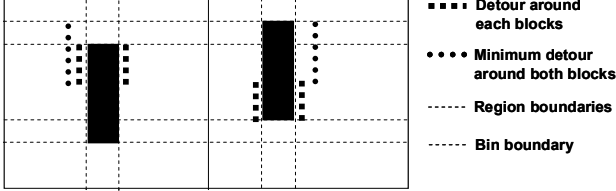


Figure 7: Horizontal adjacent bins detour with multiple blockages

To tackle this problem, first we enumerate all the regions generated by blockages as shown in Figure (7). If we have  $n$  blockages, the number of these regions equal to  $(2n + 1)^2$  since every blockages has two border lines in each direction which generates  $(2n + 1)$  regions in that direction. The main problem happens for the terminals inside the regions which located on the overlapping parts of two or more blockages in either  $X$  or  $Y$  spans. For these regions we use a trick to transform them to the standard horizontal or vertical detour problems.

**Algorithm 1.** As shown in Figure (8) for regions  $A$  and  $B$ , we cut them into two parts using a dashed line. We define the detour between  $(A_1, B_1)$  to be equal to minimum of the detours of the top and bottom part of the dotted line and the addition of the detours for all the blocks generating these two regions. All these detours can be solved using the formula (22). Similar type of analysis holds for terminals in  $(A_2, B_2)$ ,  $(A_2, B_1)$  and  $(A_1, B_2)$ . Since the number of regions to consider is large, we perform the complete calculation for the detour of  $\theta\%$  biggest blockages and add up the detour of the rest. By adjusting  $\theta\%$ , we can tune the accuracy and run time trade-off. In our experiments, we picked  $\theta=10$ .

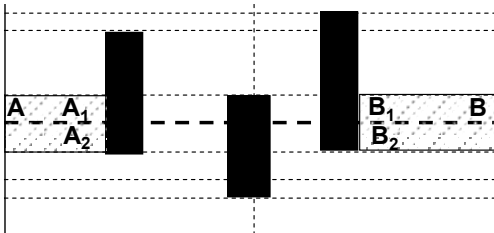


Figure 8: Algorithm 1 for detour with multiple blockage

In [3], the authors investigated the detour wirelength for the case that there is one big single blockage and numerous small blockages. There, they showed that the average detour wirelength is strongly correlated with the geometrical parameters of the big blockage such as width, height, displacement and aspect ratio, and is not related to the geometrical parameters of other small blockages. This motivates us to estimate the detour wirelength for these types of circuits by just considering the big blockage and ignoring the small blockages using the exact method presented in the previous section. But if all the blockages are of the same size, the exact method in previous section does not work and we use the heuristic presented in this section.

The analysis for the transparent-block and detour parts of the wirelength would be the same for vertically-adjacent and diagonally-adjacent bins and are so omitted from this discussion for brevity.

## 4.2 Average Wirelength

Having had the average inter-bin wirelength for horizontally, vertically and diagonally adjacent bins, the average inter-bin

wirelength can be obtained for every level of hierarchy  $h$  like in [1]. For every level of hierarchy, shown in Figure 3, the average inter-bin wirelength can be written as,

$$\bar{L}_{\text{inter},h} = \frac{1}{6} \left( \delta(L_{\text{inter}}^h(A,B) + L_{\text{inter}}^h(C,D) + L_{\text{inter}}^v(A,C) + L_{\text{inter}}^h(B,D)) \right) + (1-\delta)(L_{\text{inter}}^d(A,D) + L_{\text{inter}}^d(B,C)) \quad (25)$$

where  $h$ ,  $v$ , and  $d$ , respectively, denote that the corresponding bins are horizontally, vertically, or diagonally adjacent. Moreover,  $\delta$  is a parameter to capture the optimization behavior of placement algorithm which favors horizontally and vertically adjacent bins to diagonally adjacent bins. Placement algorithms try to minimize the length of wires as much as possible. So, the probability of having a short wire is more than having a long wire. That necessitates us to differentiate between horizontally/vertically adjacent bins and diagonally adjacent bins. To compute  $\delta$ , we use the equation derived in [2, 7] for wire length distribution for the entire circuit. In [2] by using simple theoretical considerations it is shown that the normalized wirelength distribution  $\mathcal{E}_l$  for a good two-dimensional placement is of the form of,

$$\mathcal{E}_l = Cl^{-\gamma} \quad (1 \leq l \leq l_{\max}) \\ \approx 0 \quad (l \geq l_{\max}) \quad (26)$$

which  $\gamma$  is related to Rent Exponent through equation,

$$2P + \gamma = 3 \quad (27)$$

and  $l_{\max}$  is a constant directly related to the size of the bin. This formula indicates that the number of wires with length  $l$  is decreasing with the factor of  $l^{(2P-3)}$  by increasing the length of the wire. Similar to [1], if we consider  $\mathcal{E}_{h/v}$  as the wirelength distribution between horizontal or vertical bins, and  $\mathcal{E}_d$  as the wirelength distribution between diagonal bins, we have,

$$4\mathcal{E}_{h/v} + 2\mathcal{E}_d = 1 \quad (28)$$

Since the relationship between length of the horizontal/vertical wires  $l_{h/v}$  and diagonal wires  $l_d$  for the bin configuration in Figure 3 is as  $l_d = \sqrt{2}l_{h/v}$ , we can extract the length distribution  $\mathcal{E}_{h/v}$ , and  $\mathcal{E}_d$  from,

$$4\mathcal{E}_{h/v} + 2(\sqrt{2})^{2P-3} \mathcal{E}_{h/v} = 1 \\ \mathcal{E}_d = (\sqrt{2})^{2P-3} \mathcal{E}_{h/v} \quad (29)$$

and,

$$\delta = 4\mathcal{E}_{h/v} \quad (30)$$

## 5. Experimental Results

We have implemented the techniques proposed in sections 3 and 4 in C. We compared our wirelength estimation method with the method in [1], Cheng wirelength estimation method [3], and the actual wirelength of the circuit after the routing. For placement and routing, we used the Magma BlastFusion which is a commercial CAD tool.

For doing simulations, we considered both medium and large size circuits. In order to verify our theoretical results, on the real-world circuits, we picked most of our benchmarks from the ISPD 2005 placement benchmark suite [13]. Bigblue3 is not used since it has several movable macros which should go through a process of floorplanning to fix the macros for running the estimation algorithms on it. So we excluded this benchmark from the experiments. Bigblue4 is a very huge benchmark and we couldn't run them on our available systems.

The file format of ISPD suite benchmarks is Bookshelf. The Magma BlastFusion tool accepts LEF/DEF format. We used the converter from [15] to convert the Bookshelf format to the LEF/DEF format to route the benchmarks with this tool.

For the first set of experiments we used the benchmarks with just a big single IP block. To adapt the benchmarks to our

experimental purpose, we kept the biggest blockage and changed all the other blockages to standard cells. The second set of experiments is for estimating wirelength in the presence of multiple blockages. For this set of experiments we used the original circuits from ISPD 2005 benchmark suite. The number of cells and nets in each of these test circuits are shown in Table 1. The number of fixed cells is the number of obstacles inside the chip area, and does not include the fixed I/O terminals. The utilization is the percentage of area of standard cells over the non-blocked area of chip.

For extracting Rent's exponent for each benchmark, we used the same method as [5] by performing a global placement of the benchmarks using the Dragon placement tool [14] which is an academic placement tool based on hierarchical min-cut partitioning with terminal propagation.

Table 1: Specification of the Benchmarks

Test Circuit	#Cells	#Fixed Cells	#Net	Utilization (%)	Blocked Area (%)
Test3	12,997	3	13,865	61.62	8.3
Adaptec1	211447	63	211447	57.32	43
Adaptec2	255,023	159	266,009	55.7	61.5
Adaptec3	451,650	723	466,758	33.64	61.4
Adaptec4	496045	1329	515951	27.22	48.6
Bigblue1	278164	32	284479	44.67	17.2
Bigblue2	557866	23083	577235	37.84	38.2

Table 1 shows the total wirelength estimation in presence of a single blockage for Cheng's method, the method presented in [1] and our method. Actual wirelength is reported by BlastFusion tool after the placement and routing. Table 2 illustrates the same data for wirelength in presence of multiple blockages.

As it was shown in [1], the reason that Cheng's estimation is far from actual wirelength on the circuits with high complexity is that it only considers the geometrical characteristics of the circuit toward estimating wirelength at the top level and ignores the complexity of the circuit totally. Both of the methods in [1] and our method, however, consider the complexity of the circuits into account through calculation of  $n_k$  in each level of hierarchy. As it can be seen, Cheng's method results in better estimation for the medium benchmark Test3. The reason is that on the medium-size benchmarks with lower complexity, wirelength depends more on the geometrical structure of the circuit and not on its complexity.

Table 2: Total Wirelength Estimation for Single Blockages

Circuit	Estimated WL			Actual WL
	Cheng	Method in [1]	Ours	
Test 3	3.12	4.085	2.97	2.98
Adaptec1	325.64	146.92	108.61	105.10
Adaptec2	510.71	226.76	164.60	148.90
Adaptec3	1156.84	473.39	381.29	390.55
Adaptec4	1020.99	412.15	383.60	369.29
Average Error (%)	166.04	27.65	4.09	0.0

The reason that both approaches by Cheng and [1] overestimate the wirelength is that the probability distribution of the cells on the non-blocked portion of the chip area is considered as uniform for both approaches. Placement tools try to keep the connected cells as close to each other as possible. So, the number of short wires in the chip area is more than the number of long wires after the placement. That is the reason that uniform distribution probability overestimates the length of wires, since it considers equal probability of occurrence for every length of wire. Our approach fixed this problem by considering non-uniform probability distribution for cells.

All of the three techniques perform wirelength estimation quite fast. For the largest test case Bigblue2, our method takes 85

Table 3: Total Wirelength Estimation for Multiple Blockages

Circuit	Estimated WL			Actual WL
	Cheng	Method in [1]	Ours	
Test 3	4.10	4.42	4.01	3.02
Adaptec1	366.36	197.37	148.4	156
Adaptec2	438.1	287.30	188.86	195
Adaptec3	1186.66	597.60	586.14	572
Adaptec4	1060.15	546.25	421.25	425
Bigblue1	532.50	175.50	167.43	154
Bigblue2	957.78	445.50	260.07	265
Average Error (%)	149.79	31.96	7.81	0.0

seconds, the method in [1] takes 80 seconds and Cheng method takes 75 seconds. These values include the running time for processing the input files and building the data structures.

## 6. Conclusions and Future Work

In this paper we proposed a hierarchical technique for wirelength estimation in the presence of blockages based on the assumption of non-uniform probability for the distribution of standard cells. Simulation results show that this technique estimated the wirelength much more accurately as compared to its other counterparts such as [1, 3]. The average error of this technique for large circuits is 4.09% for single blockage and 7.8% for multiple blockages. This work can be used in early design stages to provide an estimation of the end-point wirelength of a design. This method can also be extended to perform hierarchical probabilistic congestion estimation in presence of IP blocks.

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